REMARKS

Claim 57 has been amended and claims 70-72 have been added. Claims 51, 52 and 54-72 remain in the application. Reconsideration of the application is requested in view of the amendments and the remarks to follow.

The amendments to claim 57 recite Applicant's claimed subject matter with additional clarity but are not intended to alter the scope of Applicant's claims.

Claims 51, 52 and 54-69 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Koh et al., U.S. Patent No. 5,686,337; or Chan et al., U.S. Patent No. 5,627,094; or Rosner, U.S. Patent No. 5,496,757; or Kim, U.S. Patent No. 5,403,767 or Summerfelt et al., U.S. Patent No. 5,619,393. Applicant traverses for at least the following reasons.

I. Applicant's claimed subject matter.

Claim 51 recites "etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", which is not taught, disclosed, suggested or motivated by any of the cited references.

Claim 57 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings; and subsequently anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common

substrate", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 60 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 61 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming a second dielectric layer over the substrate, the second dielectric layer comprising a different material than the first dielectric layer; conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave partitions after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 62 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first

dielectric layer after forming electrically insulative partitions", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 66 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent capacitors after etching the first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions, the first and second capacitor container openings being formed on a common substrate", which is not taught, disclosed, suggested or motivated by the cited references.

The references each fail to provide the invention as recited in any of Applicant's claims. Additionally, the Office Actions fail to even attempt to relate the cited references to the invention as recited in Applicant's claims. For at least these reasons, the rejections of the claims are defective and should be withdrawn, and claims 51, 57, 60-62 and 66 and claims dependent therefrom should be allowed.

II. Unpatentability.

Unpatentability is a legal term of art. In order to make a valid finding of unpatentability, a number of legal concepts must be simultaneously satisfied.

A simple test for determining if elements suitable for a prima facie finding of unpatentability are present is set forth, for example, in the Manual of Patent Examination Procedure at §706.02(j), in a subsection entitled

"Contents of a 35 U.S.C. 103 Rejection." This MPEP section states, among other things, that all of the elements of the claims must be found in the prior art in order to find unpatentability. As noted above in section (I), the references fail to provide all of the elements recited in Applicant's claims. As a result, the proposed combination does not and cannot provide the invention as recited in any of Applicant's claims and thus cannot render Applicant's claims unpatentable.

Accordingly, the rejection of claims 51, 52 and 54-69 is plainly defective and should be withdrawn, and claims 51, 52 and 54-69 should be allowed.

IIA. Lack of demonstration of motivation or suggestion.

Baldly mischaracterizing or mis-stating teachings from references or modifying or augmenting teachings from one or more references, without demonstrating any relationship to the pending claims, does not meet appropriate standards for a rejection under 35 U.S.C. §103(a). The prosecution history in the present application does no more than nakedly list various things purportedly taken from the references. There is no showing in the record of how these elements could possibly correspond to the subject matter recited in any of Applicant's claims, of how the teachings of the references could be modified or why one would do so.

Appropriate standards for a prima facie finding of unpatentability are set forth in The Manual of Patent Examination Procedure at §706.02(j), in a subsection entitled "Contents of a 35 U.S.C. 103 Rejection" and are also discussed in MPEP §2142, entitled "Legal Concept of Prima Facie

Obviousness". These MPEP sections state that three basic criteria must be met in order to establish a prima facie case of obviousness.

The first of these is that there must be some motivation to combine or modify teachings of the references. There is no motivation identified anywhere to modify the references to attempt to arrive at the subject matter of Applicant's claims.

As a result, the proposed combination does not and cannot provide the invention as recited in any of Applicant's claims and thus cannot render Applicant's claims unpatentable.

The Office Action fails to show that the subject matter of any of claims 51, 52 and 54-69 is suggested or motivated by the teachings of any of the references. In fact, the Office Action is silent with respect to any reason to modify the teachings of any of the references. Put another way, the Examiner has not provided evidence of any shred of such motivation or suggestion, or, for that matter, modification of teachings, anywhere in the entire prosecution history!

For at least these reasons, the rejection of claims 51, 52 and 54-69 is improper and should be withdrawn, and claims 51, 52 and 54-69 should be allowed.

IIB and C. Lack of expectation of success and of recited elements.

The second requirement of MPEP §§706.02(j) and 2142 is that there must be a reasonable expectation of success. The third requirement is that

the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

IIC(i). Koh et al.

IIC(i)(a). Koh et al. are silent with respect to forming an insulator intermediate two etching acts, as recited in claims 51, 60-62 and 66, or first and second anisotropic etching acts, as recited in claims 57, 60-62 and 66. As such, the teachings of Koh et al. cannot possibly provide the invention as recited in any of Applicant's claims. As a result, there cannot possibly be a reasonable expectation of success from modifying the teachings of the Koh et al. reference.

Koh et al. teach "A one mask/four etch step process to form a curved storage node for an advanced DRAM cell capacitor." (Abstract). This process includes several steps.

Koh et al. teach (Fig. 2) a first isotropic etch to form all of the capacitor container openings (col. 2, lines 27-35; col. 5, lines 30-51). Alternatively, in the embodiment of Fig. 3, a "starter hole" is anisotropically etched (col. 2, lines 54-61; col. 6, lines 4-24), followed by the isotropic etch. In the various embodiments taught by Koh et al., all of the capacitor container openings are etched at the same time and in the same steps, in contrast to Applicant's claimed process.

Koh et al. teach (col. 2, lines 36-40) that "As shown in FIGS. 2 and 5 in the first isotropic etch, the first dielectric layer 30 is isotropically etched through the first opening 36 in the resist layer 34 forming the electrode hole

31." Koh et al. also teach (col. 5, lines 47 and 48) that "The isotropic etch forms projections 30A of the first planarization layer." Koh et al. teach formation of the projections 30A from the planarization dielectric 30 in a first isotropic etching step employed to etch all of the capacitor containers.

In a third embodiment described with reference to Figs. 6A and 7, Koh et al. teach (col. 7, line 18 et seq.) masking of the peripheral area followed by blanket isotropic etching of dielectric layer 44 and dielectric layer 30 (col. 7, lines 7 and 23-25) to leave the dielectric portion 30B from the previously-deposited dielectric layer.

Accordingly, the Examiner's characterization (p. 4) of the teachings of Koh et al. (to the effect that the insulator 30A is "formed between two capacitors after second etching in fig. 5 or fig. 7" is in error. Additionally, the statement at p. 2 to the effect that Koh et al. teach "forming an insulative partition 30a between the capacitor container with anisotropic etching, fig. 7" is in error.

The discussion referencing Fig. 7 in Koh et al. (col. 6, line 64 through col. 7, line 10) indicates that this is a selective etch, i.e., etches a first planarization layer 44 more rapidly than it etches doped first dielectric layer 30 (col. 7, lines 11-17). This is not an anisotropic etch and is not arbitrarily interchangeable with such.

The discussion of the specific etch chemistry (col. 7, line 8) indicates that this is a wet HF etch. In other words, this is an isotropic etch, and is not an anisotropic etch as mistakenly alleged in the Office Action

Additionally, the Examiner fails completely to address the recitations of anisotropic etching in any of Applicant's claims 52, 55-57, 60-63, 66, 68 and 69. Koh et al. do not provide teaching or disclosure of such anisotropic etching.

Further, Koh et al. fail to teach, disclose, suggest or motivate forming the partitions by forming insulative material and conducting an anisotropic etch, as recited, in varying language, in claims 52, 63, 68 and 69.

The rejection of independent claims 51, 52, 55-57, 60-63, 66, 68 and 69 as being unpatentable over Koh et al. fails all three components of the test for an obviousness rejection as set forth in the MPEP. For at least these reasons, the rejection of claims 51, 52, 55-57, 60-63, 66, 68 and 69 should be withdrawn, and claims 51, 52, 55-57, 60-63, 66, 68 and 69 should be allowed.

IIC(i)(b). Examiner's admission on the record regarding Koh et al.

The Examiner's rejection based on the teachings of the teachings of Koh et al. demonstrates on its face that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claims 51, 52, 55-57, 60-63, 66, 68 and 69. The Examiner indicates (p. 2) that the etching acts are shown in Figs. 3 and 5, while the insulative partitions are shown in Fig. 7, corresponding to a processing act subsequent to both of the etching acts. The Examiner restates this in the Conclusion (p. 3), noting that "Koh et al. clearly teaches an insulating layer formed between two capacitors after second etching."

To clarify this further, forming of a partition subsequent to two etching acts, as allegedly shown by Koh et al., is not equivalent to "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", as positively recited in claim 51. In other words, Koh et al. do not teach, disclose, suggest or motivate "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", and the Examiner fails to show any such step in Koh et al.

In fact, the Examiner's *Conclusion* in the Office Action dated June 26, 2001, and in the Final Office Action dated June 14, 2002, reiterates that Koh et al. do not teach or disclose the invention as recited in claim 51. The Examiner states (p. 4) that "Koh et al. clearly teaches an insulating layer formed between two capacitors after second etching." This is a repeated, explicit admission, on the record, that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claim 51.

In contrast, claim 51 recites "etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps".

Applicant specifically points out for the Examiner's benefit that teaching that something occurs after two etching steps does not teach something that occurs intermediate two etching steps. The word "intermediate" means "between", and does not mean or include "after".

To clarify this point yet further, a copy of p. 611 of the Merriam Webster's Collegiate Dictionary, 10TH Ed. (Merriam Webster, Springfield MA,

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copyright 1993), was enclosed in an Information Disclosure Statement together with the last Response. This page includes a definition of intermediate, viz., "beginning or occurring at the middle place, stage, or degree or between extremes". As such, it is abundantly clear that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claim 51. For at least these reasons, the rejection of claim 51 based on the teachings of Koh et al. is defective and should be withdrawn, and claim 51 should be allowed.

Claim 57 recites plural anisotropic etching steps. Koh et al. teach a first embodiment with respect to Figs. 2 and 5 using (col. 5, lines 36-40) using one isotropic etching step, followed by one anisotropic etch of the same structure. Koh et al. not only fail to teach plural anisotropic etching steps, Koh et al. also do not teach etching of first and then second capacitor container openings, as recited in claim 57.

To clarify these concepts, Applicant has provided copies of pages 46 and 622 of Merriam Webster's Collegiate Dictionary, 10^{TH} Ed. (Merriam Webster, Springfield MA, copyright 1993), in an Information Disclosure Statement that was included together with the last Response. The definition of "anisotropic" is "exhibiting properties with different values when measured in different directions". An anisotropic etch is an etch having a higher etch rate in one direction than in another within a single material.

The definition of "isotropic" is "exhibiting properties (as the velocity of light transmission) with the same values when measured along axes in all

directions". An isotropic etch is an etch exhibiting the same etch rate in all directions (see, e.g., the dashed line in Fig. 3 of the Koh et al. reference).

Koh et al. teach a second embodiment with respect to Fig. 3 (see col. 6, line 4 et seq.). The second embodiment also fails to teach etching of first and then second capacitor container openings, as recited in claim 57. Koh et al. also do not teach first and second anisotropic etching steps with respect to the second embodiment. For at least these reasons, the rejection of claim 57 based on the teachings of Koh et al. is clearly defective and should be withdrawn, and claim 57 should be allowed.

Similarly, claims 60-62 and 66 provide an explicit ordering of etching, forming partitions and then, following formation of the partitions, second etching. Again, the Examiner's own conclusion shows clearly that Koh et al. cannot possibly provide the invention as recited in these claims. For at least these reasons, the rejection of claims 51, 52, 55-57, 60-63, 66, 68 and 69 based on the teachings of Koh et al. are clearly defective and should be withdrawn, and claims 51, 52, 55-57, 60-63, 66, 68 and 69 should be allowed.

IIC(ii). Chan et al.

Chan et al. teach formation of a patterned planarized first dielectric layer 20b in a first anisotropic etching step (Fig. 2b; col. 8, lines 25-35). This step also defines all of the capacitor container openings. As a result, Chan et al. do not and cannot teach, disclose, suggest or motivate the invention as recited in claims 51, 60-62 and 66.

More specifically, Chan et al. teach formation of an insulator 20 (Fig. 2a). A patterned mask layer 24b is then formed (Fig. 2b; col. 7, lines 11-17). The insulator 20 is then etched to form dielectric layer portion 20b (Fig. 2b). The patterned portion 22b of the second dielectric layer is then completely etched (Fig. 2c and col. 8, line 57 through col. 9, line 6).

Because the dielectric layer portion 20b is formed during the first etching step and thus is shown clearly in Fig. 2b, it cannot be the result of "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", as recited in claim 51.

Claim 57 recites first and second anisotropic etching steps. The second etching step taught by Chan et al. is an isotropic etching step (col. 8, lines 61 and 62). The undercutting needed to remove the portion 24b cannot be carried out using anisotropic etching. Similarly, claims 60-62 and 66 provide an explicit ordering of anisotropic etching, forming partitions and only then, following formation of the partitions, second anisotropic etching.

As a result, Chan et al. do not and cannot teach, disclose, suggest or motivate the invention as recited in claims 51, 57, 60-62 and 66. Because Chan et al. fail to provide the elements recited in Applicant's claims, there can be no reasonable expectation of success from modification of Chan et al. to attempt to arrive at Applicant's claimed subject matter. The rejection based on Chan et al. fails all three prongs of the test for unpatentability found in the MPEP.

The Examiner states (p. 4) that "Chan clearly teaches anisotropical etching first capacitor container opening (left hand side) and anisotropical

etching second capacitor container (right hand side) with an insulative partition 20b on a common substrate 10 in fig. 2b. (meeting claims 57-69)."

This is not the same as the ordered sequence of acts that are recited in Applicant's claims as described above to form first capacitor containers, an insulative partition and then second capacitor containers.

For at least these reasons, the rejections of claims 51, 57, 60-62 and 66 based on the teachings of Chan et al. are defective and should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

IIC(iii)(a). Rosner.

Rosner does not teach or disclose formation of an insulative partition intermediate two etching steps, as recited in claim 51. Additionally, Rosner teaches (col. 5, lines 54 and 55) that, with reference to Fig. 4, "The first auxiliary layer 4 is then removed by wet-chemical etching using, for example, choline." Wet etching of polysilicon layer 4 (col. 5, line 17) is, by definition, isotropic etching. Accordingly, Rosner does not teach first and second anisotropic etching acts, as is recited in each of claims 60-62 and 66.

Claim 57 recites first anisotropic etching first capacitor container openings and subsequent anisotropic etching of second capacitor container openings. Claims 60-62 and 66 each clearly recite an ordered sequence of acts such as (i) anisotropic etch to form first capacitor containers, (ii) formation of insulative partitions and (iii) anisotropic etch to form second capacitor containers. In contrast, the Examiner's bald recitation of teachings

from Rosner indicates that Rosner teaches an ordered sequence of acts such as (i) etch, (ii) isotropic etch and subsequent (iii) insulator formation.

The Examiner states (p. 3) that Rosner teaches "etching insulating layer 4 to form a capacitor container in first etching step fig. 3". The Examiner is mistaken.

Rosner teaches (col. 5, lines 26-40) formation of openings 6 and layers 7 and 8 that subsequently form insulative partitions between capacitors. A "capacitor container" is a container that holds a capacitor. The openings 6 clearly are not capacitor containers.

The Examiner states (p. 3) that Rosner teaches "etching (removing) insulating layer 4 to form a capacitor container in second etching step". Rosner teaches (col. 5, line 54 et seq.) a single wet etching step to remove the layer 4 and to form all of the capacitor containers. This is different from (and thus is not the same as) the invention as recited in any of Applicant's claims.

The Examiner states (p. 3) that Rosner then teaches "forming an insulative partition 81 between the capacitor container, fig. 6." This is an admission that Rosner does not teach formation of the insulative partition between formation of the first capacitor containers and formation of the second capacitor containers, as recited in Applicant's claims.

Additionally, claims 52, 61, 63, 68 and 69 each explicitly recite formation of the insulative spacer via an anisotropic etching act. Claims 61. 63, 68 and 69 each clearly recite an anisotropic etching act for formation of the insulative spacer in addition to the two separate anisotropic etching acts

for forming the first and second capacitor containers, viz., recite three anisotropic etching acts. No such teaching has been identified in Rosner.

Further, the Office Action does not contain any statement or effort to relate this disclosure to the subject matter of any of Applicant's claims. As a result, Rosner does not and cannot teach, disclose, suggest or motivate the invention as recited in claims 57, 60-62 and 66.

Because Rosner fails to provide all of the affirmatively-recited acts of Applicant's claims, there cannot possibly be a reasonable expectation of success from modification of the teachings of the Rosner reference. The rejection of claims 51, 52, 57, 60-62, 66, 68 and 69 fails all three components of the test for unpatentability set forth in the MPEP.

For at least these reasons, the rejection of claims 51, 52, 57, 60-62, 66, 68 and 69 based on the teachings of the Rosner reference is defective and should be withdrawn, and claims 51, 52, 57, 60-62, 66, 68 and 69 should be allowed.

IIC(iii)(b). Examiner's admission on the record regarding Rosner.

The Examiner's rejection (p. 3) based on the teachings of Rosner demonstrates on its face that Rosner does not teach, disclose, suggest or motivate the invention as recited in any of claims 51, 57, 60-62 and 66. The Examiner indicates (p. 3) that the etching acts are shown in Figs. 3-5, while formation of the insulative partition is shown in Fig. 6, corresponding to a processing act subsequent to the etching acts. In contrast, Applicant's claims recite an ordering of acts whereby first capacitor containers are formed and

then second capacitor containers are formed, or whereby first capacitor containers are formed, an insulative partition is formed and then second capacitor containers are formed.

For at least these reasons, the rejection based on Rosner is clearly defective and should be withdrawn, and claims 51, 57, 60-62 and 66 and claims dependent therefrom should be allowed.

IIC(iv). Kim.

The Examiner states (p. 3) that Kim teaches etching insulating layer 7 to form a capacitor container in first etching step fig. 1C. The Examiner is mistaken.

Kim teaches etching first openings in an insulating layer 7 in Fig. 1C. The first openings are not capacitor container openings. The first openings are clearly formed at a location that eventually is between the locations in which capacitors are later formed (see Fig. 1F). The process associated with Fig. 1C results in formation of insulative structures 7A in the locations that will later hold capacitors. Insulative patterns in the form of right cylindrical structures (col. 2, lines 33-37) are not capacitor containers or capacitor container openings. Spaces formed between such insulative structures also are not capacitor containers or capacitor container openings.

Kim then teaches formation of second insulating film spacers 8A followed by formation of "etching barrier layer 9" (Fig. 1D; col. 2, lines 42-57). Kim teaches (col. 2, line 62 et seq.) formation of all of the capacitor containers in Fig. 1E by removal of the reminder of the insulating layer 7A

and the insulating spacers 8A in a single etching step. Kim is silent as to how this etching step is carried out. Kim does not teach formation of first and second capacitor containers by first and second anisotropic etching acts, as is affirmatively recited in each of Applicant's claims 55-57, 60-62 and 66. Additionally, Kim does not teach formation of an insulative barrier by yet another anisotropic etching act, as is affirmatively recited in claims 61, 63, 68 and 69. Kim is silent as to how the etching referenced with respect to Figs. 1E and 1F is carried out.

As a result, Kim does not and cannot teach, disclose, suggest or motivate formation of insulative partitions between two separate etching steps, as recited in claims 51, 60, 61, 62 and 66.

Further, because Kim does not teach anisotropic etching until Fig. 2A (col. 3, lines 37-44), the cited portions of Kim cannot possibly teach, disclose, suggest or motivate the invention as recited in any of claims 57, 60-62, 66, 68 and 69. Because Kim fails to provide the elements recited in Applicant's claims, there can be no reasonable expectation of success from modification of Kim to attempt to arrive at Applicant's claimed subject matter. The rejection based on Kim fails all three prongs of the test for unpatentability found in the MPEP.

For at least these reasons, the rejection of claims 51, 55-57, 60-62, 66, 68 and 69 based on the teachings of Kim is defective and should be withdrawn, and claims 51, 55-57, 60-62, 66, 68 and 69 should be allowed.

IIC(v). Summerfelt et al.

The Examiner first makes reference to Figs. 25+ and then states that Summerfelt teaches etching insulating layer 70 in Fig. 25. The Examiner is mistaken.

Figs. 24-32 are discussed in the specification, beginning at col. 8, line 36. Summerfelt teaches (col. 8, lines 53-56) that "TiN capacitor plugs 52 are again formed in SiO_2 insulator 32 as shown in FIG. 24, then SiO_2 pillars are formed over TiN plugs 52." Summerfelt et al. are silent as to how these pillars 70 are formed. There is no teaching of etching of any layer 70 as erroneously alleged in the Office Action.

Because the remainder of the Examiner's discussion of Summerfelt et al. is incomprehensible and again makes reference to Fig. 1E, which is not present in Summerfelt et al., Applicant will describe what Summerfelt et al. do teach.

Summerfelt et al. teach formation of what will later become capacitor dielectric layers 56 using BST (barium strontium titanate) in Figs. 25-28 (see also col. 8, line 36 through col. 9, line 8). In particular, the capacitor dielectric layer 56, apparently relied on by the Examiner to provide Applicant's recited insulative partition, is formed with reference to Figs. 26 and 27.

The material 70 is etched with reference to Fig. 28, after the formation of the BST pillars 56. Summerfelt et al. teach (col. 8, line 60 et seq.) that the BST formation process is highly oxidizing and that the material 70 functions as an oxidation barrier. As a result, Summerfelt et al. teach away from

formation of any capacitor containers by removal of the material 70 prior to formation of the BST pillars 56.

Further, Summerfelt et al. state (col. 9, lines 5-7) that the material 70 may be wet or dry etched. Accordingly, there is no teaching of anisotropic etching, as is affirmatively recited in Applicant's claims 57, 60-62 and 66, or of forming insulative partitions between adjacent capacitor containers, as recited in claims 51, 59, 60-63, 66, 68 and 69. These claims each clearly recite an ordered sequence of acts such as (i) anisotropic etch, (ii) formation of insulative partitions and (iii) anisotropic etch.

Summerfelt et al. teach that a first capacitor electrode is formed atop conductive plug 52, using a platinum layer 74 and a conductive titanium nitride layer 76 (fig. 29; col. 9, lines 8-14). Portions of these conductive layers 74 and 76 formed atop the BST pillars 56 are then removed (Fig. 31; col. 9, lines 16-21).

As a result, an outer electrode comprising platinum 60 and titanium nitride 64 is formed on an outer surface of the capacitor dielectric 56, and an inner electrode comprising platinum 58 and titanium nitride 62 is formed within an inner surface of the capacitor dielectric 56. As noted by Summerfelt et al. (col. 9, lines 26-28), "As can be seen in FIG. 31, the outer electrode can be made common between e.g., all capacitors in a DRAM." As a result, it is apparent that the outer surface of the capacitor dielectric 56 cannot possibly form a second capacitor container, as alleged in the Office Action and as recited in Applicant's claims.

In fact, Summerfelt et al. teach methods of forming capacitors that do not employ capacitor containers. Summerfelt et al. teach methods of forming free-standing capacitors (see, e.g., cover illustration, Figs. 10-12, 19, 20, 23 and 32), i.e., capacitors formed to project from the substrate and that are not formed in containers disposed on the substrate. The capacitors of Fig. 32 comprise an outer electrode having layers of platinum 60 and TiN 64, a dielectric layer 56 formed from high dielectric constant material BST, an inner electrode having layers of platinum 58 and TiN 62 and an inner core of SiO_2. As a result, the individual capacitors are separated from one another by conductive layers comprising the outer common electrode, and not by insulative partitions, as recited in Applicant's claims.

For at least these reasons, the rejection of claims 51, 52 and 54-69 over Summerfelt et al. is clearly in error and should be withdrawn, and claims 51, 52 and 54-69 should be allowed.

Claim 57 recites "a method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings; and subsequently anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate."

Summerfelt et al. provide no teaching at all of first and second capacitor container openings. The Office Action is also silent with respect to the invention as recited in claim 57. As noted above, Summerfelt et al. do not teach formation of capacitors in containers and instead teach formation of

free-standing capacitors separated from one another by the conductive outer electrode and not by any insulative partition.

Summerfelt et al. teach anisotropic ion milling of platinum (col. 7, lines 63-65). Summerfelt et al. also teach anisotropic etching of BST to form capacitor dielectric layer 56 (col. 8, lines 56-60). Summerfelt et al. make no further mention of anisotropic etching. As a result, it is inconceivable that Summerfelt et al. could possibly teach, disclose, suggest or motivate the multiple anisotropic etching steps recited in each of claims 57, 60-62 and 66.

Because Summerfelt et al. fail to provide the elements recited in Applicant's claims, there can be no reasonable expectation of success from modification of Summerfelt et al. to attempt to arrive at Applicant's claimed subject matter. The rejection based on Summerfelt et al. fails all three prongs of the test for unpatentability found in the MPEP.

For at least these reasons, the rejection of claims 51, 57, 60-62 and 66 is in error and should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

III. Modification cannot defeat intended purpose.

Attempting to adapt the teachings of Chan et al. to arrive at the subject matter recited in claims 57, 60-62 and 66 defeats the main intent of Chan et al. and also makes the teachings of Chan et al. unsuitable for their intended purposes. It is improper to modify the teachings of a reference in such a manner (see MPEP §§ 2145(X), 2141.02 and 2143.01).

More specifically, the second etching step taught by Chan et al. is an isotropic etching step (col. 8, lines 61 and 62). The undercutting needed to remove the portion 24b cannot be carried out using anisotropic etching. Claim 57 recites first and second anisotropic etching steps. Similarly, claims 60-62 and 66 provide an explicit ordering of anisotropic etching, forming partitions and then, following formation of the partitions, second anisotropic etching.

Because substitution of Applicant's affirmatively-recited acts into the teachings of Chan et al. renders it impossible to achieve the undercutting needed by Chan et al., the teachings of Chan et al. are rendered unsuitable for their intended purpose if modified to arrive at Applicant's claimed subject matter. Such also defeats the main intent of Chan et al.

Applicant notes the requirements of MPEP §2143.01, entitled "Suggestion or Motivation to Modify the References". This MPEP section states that "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE". This MPEP section further states that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)."

Accordingly, there is no suggestion or motivation, as a matter of law, to modify the teachings of Chan et al. to attempt to arrive at the subject matter of any of Applicant's claims. For at least these reasons, the rejection of

claims 57, 60-62 and 66 should be withdrawn, and claims 57, 60-62 and 66 should be allowed.

IV. Dependent claims.

Dependent claims 52, 54-56, 58, 59 and 63-65 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

For example, claim 55 recites that "etching capacitor container openings comprises: anisotropically etching first capacitor container openings in a first etching step; and anisotropically etching second capacitor container openings in a second etching step", while claim 56 recites that "etching capacitor container openings comprises: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings", which is not taught, disclosed, suggested or motivated by any of the cited references, and which further appears nowhere in the Office Action.

V. Lack of Evidence for motivation.

Further, no evidence has been provided as to why it would be obvious to modify the teachings of any of these references. Evidence of a suggestion to combine or modify may flow from the prior art references themselves, from the knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

No motivation for modifying the teachings of the references is provided in the Office Action. In fact, no modifications are proposed. The rejections merely mischaracterize and misrepresent the teachings of the references. For at least these reasons, the rejection of claims 51, 52 and 54-69 should be withdrawn, and claims 51, 52 and 54-69 should be allowed.

VI. Plain meaning.

Applicant notes that the interpretation the Examiner seems to be placing on the teachings of the references appears to construe any opening formed in conjunction with formation of capacitors as a "capacitor container". This contravenes the plain meaning of the terms forming the phrase "capacitor container" and is also at odds with the discussion in Applicant's specification of formation of capacitor containers (starting at p. 11, line 11). It is improper to give terms in a claim a meaning repugnant to the ordinary meaning of the terms, as is explained below in more detail with reference to MPEP §608.01(o), entitled "Basis for Claim Terminology in Description".

This MPEP section states that "The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import; and in mechanical cases, it should be identified in the descriptive portion of the specification by reference to the drawing, designating the part or parts therein to which the term applies. A term used in the claims may be given a special meaning in the description. No term may be given a meaning repugnant to the usual meaning of the term."

As defined in Merriam Webster's Collegiate Dictionary, 10TH Ed. (Merriam Webster, Inc., Springfield MA, principal copyright 1993) on page 249 (copy enclosed), the term "container" means "one that contains; *esp.* a receptacle (as a box or a jar) for holding goods". Accordingly, a "capacitor container" would be a "receptacle" for holding a "capacitor". The definition that the Examiner appears to be employing is repugnant to this interpretation of the term "capacitor container" and thus is improper.

The Examiner also appears to be conflating several terms of art to describe different types of etching techniques employed in the semiconductor arts. As noted above, isotropic etching, such as many types of wet chemical etching and some types of plasma etching, etches equally rapidly in all directions. An example of the term "isotropic etching" is given in Koh et al. at col. 5, line 36 et seq. and the effects of such etching are shown in Fig. 2 by dashed lines and arrows.

This is not the same as or arbitrarily interchangeable with anisotropic etching. Anisotropic etching is typically plasma etching that takes place under circumstances intended to promote etching more rapidly in one direction than in another direction. An example of the term "anisotropic etching" is given in Koh et al. at col. 6, lines 4 et seq. and the effects of anisotropic etching are illustrated by the rectangular outline below the opening 36. This passage illustrates that anisotropic etching followed by isotropic etching can achieve results that neither approach alone is capable of, i.e., that these are different processes and are not arbitrarily

interchangeable. Another example of anisotropic etching appears in Chan et al. with reference to Fig. 2B at col. 8, line 29 et seq.

Additionally, selective etching refers to etching one material more rapidly or more slowly than another material (see, e.g., Koh et al., col. 7, lines 2-4 for an example of this term of art as it is employed in the relevant arts). Selective etching is different from, and not arbitrarily interchangeable with, anisotropic etching.

None of these forms of etching necessarily implies another of these forms of etching, and these types of etches are not arbitrarily interchangeable. In fact, the passage in Koh et al. at col. 5, line 36 et seq. illustrates that an etch having isotropic properties may also be chemically selective, that is, etch different materials at different rates (see esp. lines 42-46). Another example of isotropic selective etching is provided in Chan et al. at col. 8, line 61 et seq. with reference to Fig. 2C. Chan et al. provide a definition of isotropic selective etches at col. 9, line 7 et seq. These examples should serve to illustrate that such terms are used with particularity in the relevant arts and that they are not interchangeable.

Accordingly, in reading and interpreting the references, it is important to recognize that different types of etching are employed for different reasons in each situation. These types of etches usually are not interchangeable, as it would appear the Examiner is employing these terms. If the Examiner is of the opinion that one type of etch might be exchanged for another, the Examiner needs to provides reasons why this is appropriate, why the prior art

suggests or motivates such modification and why such would not render the prior art or the claimed subject matter unsuitable for its intended purpose.

For at least these reasons, the unpatentability rejections are in error and should be withdrawn, and claims 51, 52 and 54-72 should be allowed.

VII. Examiner deficiencies.

The Examiner's response to argument is deficient in multiple regards. Additionally, several formal matters have not been addressed. This is explained below in more detail.

VII(i). A first deficiency is that the response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §103, or, in the alternative, is an admission that these rejections are defective.

Applicant notes the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites 37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented

by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated.

VII(ii). A second deficiency is that under the unpatentability rejections, the combinations fail to provide all of the features recited in any of Applicant's independent claims (see MPEP §§706.02(j) and 2142 for criteria for establishing a prima facie case of unpatentability). The Examiner has ignored these features without providing any appropriate legal basis for doing so.

For example, the Examiner states (p. 4) that "Rosner, Kim and Summerfelt also clearly teaches first and second anisotropical etchings to form an insulative partition as set forth above and meeting claims 57-69." Applicant's claims do not recite first and second anisotropic etchings to form an insulative partition, rather, they recite such etchings to form first and second capacitor containers.

Additionally, claims 52, 61, 63, 68 and 69 each explicitly recite formation of the insulative spacer via an anisotropic etching act. Claims 61. 63, 68 and 69 each clearly recite an anisotropic etching act for formation of the insulative spacer in addition to the two separate anisotropic etching acts for forming the first and second capacitor containers, viz., these claims recite

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three anisotropic etching acts. No such teaching has been identified in any of the references.

VII(iii). A third deficiency is the failure to respond to all arguments traversing the unpatentability rejections. Merely repeating or mischaracterizing various elements taught by the references does not constitute a basis for rejection of the claims. This is particularly true when the references fail to provide the features recited in the claims and the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

VII(iv). A fourth deficiency is the failure to return initialed form PTO-1449 forms to Applicant. Specifically, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed in this application on September 26, 2001, and again on April 11, 2002, together with the last Response. No initialed copy of the PTO-1449 has been received back from the Examiner.

To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

VII(v). A fifth deficiency is a failure to advise Applicant of the status of the drawings. Formal drawings were filed in this Application on October 21, 1999.

None of the four Actions to date have provided any indication of the status of the drawings. Clarification is again requested.

For at least these five reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments.

In order to assist the Examiner in identifying the arguments in order to respond to them, Applicant has specifically enumerated them. The Examiner should either allow Applicant's claims or provide meaningful rebuttal to each of arguments **I, II, IIA, IIC(i)(a), IIC(i)(b), IIC(ii), IIC(iii)(a), IIC(iii)(b), IIC(iv), IIC(v), III, IV, V, VI** and **VII(i)-(v)**, which the Examiner has improperly ignored. In fact, no aspect of the Office Action, including the Examiner's response to argument, provides any credible evidence that the Examiner has even read Applicant's arguments.

New claims 70-72 are supported at least by page 6, line 2 through page 18, line 9 of the application as originally filed. No new matter is added by new claims 70-72. New claims 70-72 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 51, 52 and 54-72 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Sept. 16, 2002 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

OIPE
SEP 16 2002
PATENT & TRADEMARK OFFICE
JC67

Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/420,635
Filing Date ..... October 21, 1999
Inventor ..... Werner Juengling
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... H. Tsai
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY
RESPONSE TO JUNE 14, 2001 OFFICE ACTION

Deletions are bracketed, additions are underlined.

57. (Amended) A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings; and

subsequently anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate.

Claims 70-72 have been added.

END OF DOCUMENT

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